Computer Architecture
ELE 475
Fall 2014
Problem Set #4
Total Points: 100

Problem #1 (20 Points): Page 136 in H&P5, Problem 2.8 parts a, b, and c.

Problem #2 (10 Points): Page 138 in H&P5, Problem 2.11 parts a and b.

Problem #3 (10 Points): What is the reach of a 16 entry fully associative TLB assuming that there are two valid page sizes, 4KB and 1MB?

Problem #4 (10 Points): You are designing the page tables for a processor with a 64-bit virtual address space. The top bit is reserved and is always set to be zero, therefore there is effective 63-bit virtual address space. The processor has a 64-bit physical address space. Assuming a page size of 8KB, construct a multi-level page table where the different levels of the page table naturally fit within an 8KB page. Assume that each leaf page table entry needs a valid bit, a dirty bit, a kernel/supervisor bit, and two software reserved bits. Assuming that the OS dedicates 10 pages to page table entries (any level) to a particular process, what is the maximum amount of physical memory that can be addressed by that process? What is the minimum?

Problem #5 (10 Points): On a machine with a software-managed memory management unit (MMU) when a TLB miss occurs, what are the possible reasons? Does this always result in a bus-error/segmentation fault? On a machine with a hardware managed MMU with hardware page-table walker, does a page fault always result in a bus-error/segmentation fault?

Problems continued on next page

Problem #6 (20 Points): You are executing on a VMIPS (as described on p. 266 of H&P5) architecture the code below. Assume that the maximum vector length of the architecture is 128. Draw the pipeline diagram of this code executing on a single-lane architecture which has an independent load unit, store unit, multiply unit, and ALU unit. Loads have a latency of three cycles (L0, L1, L2), stores take two cycles to occur (S0, S1), multiplies take 5 cycles (Y0, Y1, Y2, Y3, Y4), and ALU operations take two cycles (X0, X1). Assume full pipelining of the functional units. Assume that the pipeline has a dedicated register read stage and a single write-stage. For the first part of this problem, assume that the architecture support chaining through the register file, but only has two read ports and one write port on the register file.

```
C Code:
for (i = 0; i < 6; i++)
{
   a[i] = (b[i] * 7) + c[i];
}
```

```
VMIPS:
ADDI R7, R0, 7
CVT.W.D F2, R7
ADDI R1, R0, 6
MTC1 VLR, R1
LV V1, R4
MULVS.D V3, V1, F2
LV V2, R5
ADD V4, V3, V2
SV R6, V4
```

Problem #7 (10 Points): Redo the above pipeline diagram (Problem #6) assuming that the pipeline has a write port and two read ports per functional unit and that the architecture has two lanes (two duplicates of all functional unit resources).

Problem #8 (10 Points): Do GPUs have vector length registers? Describe how GPUs handle the case where two elements in a vector of data need different processing.