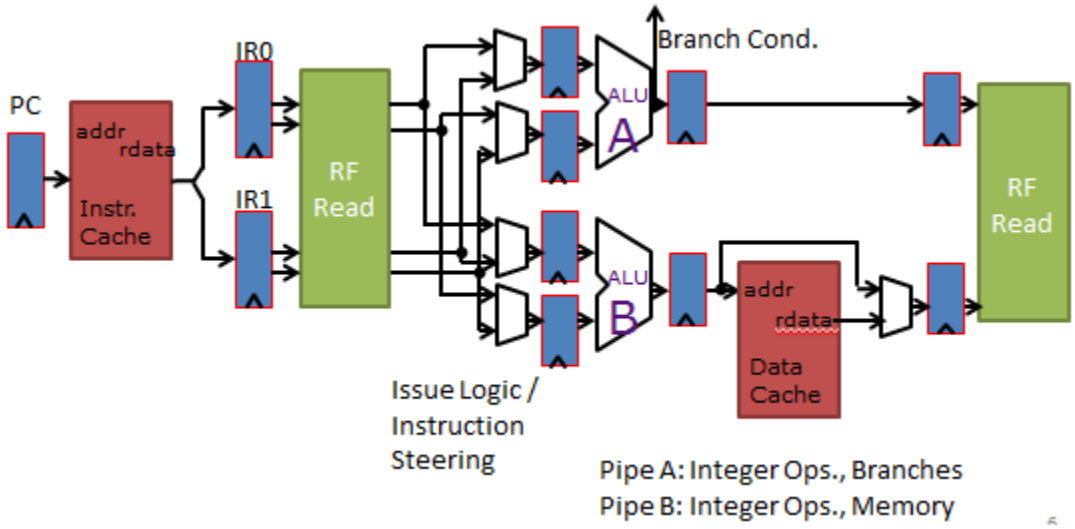
Computer Architecture
ELE 475
Fall 2014
Problem Set #2
Total Points: 100

Problem #1 (10 Points): Draw the pipeline diagram of the following code executing on the shown in-order two-way superscalar processor. Assume that branches execute in pipeline A, loads/stores in pipeline B. Assume full bypassing when possible and no alignment problems.



[Figure of Two-Wide In-order Superscalar Processor Pipeline]

ADD R5, R6, R7
SUB R6, R7, R8
LW R10, R6(0)
ADDIU R12, R13, 1
LW R15, R6(4)
LW R15, R15(4)
ADD R6, R9, R10
ADDIU R8, R10, R11

Problem #2 (20 Points): Given that you have an architecture which has the following pipeline stages:
F D I X0 X1 W
and that register fetch happens in the I stage of the pipeline and branch resolution happens in X1, how many dead instructions are need to be killed when a branch miss-predict is taken? Now assume that the pipeline is a three-wide superscalar, how many instructions need to be killed on a branch miss-predict? (Assume that the branch is the first instruction executing after a jump.)

Problem #3 (20 Points): A processor is executing code and executes a divide instruction which divides by zero.
(a)Describe in the MIPS instruction set what state needs to be saved by the hardware interrupt mechanism.
(b)Assume that the interrupt handler reads registers R5, R6, R7 and writes registers R5, R8, R10, what registers does the interrupt handler need to save.
(c)What state does the ERET instruction change?

Problem #4 (20 Points): An instruction takes the following synchronous exceptions: Instruction Address Exception and ALU Overflow. What should the interrupt cause be loaded with? What if that same instruction has an external interrupt pending? Explain why?

Problem #5 (10 Points): Assume that you have the IO2I pipeline from lecture. It can issue one instruction per cycle and can commit one instruction per cycle. Draw the pipeline diagram of the following code sequence executing.
MUL R6, R7, R8
ADD R9, R10, R11
ADD R11, R12, R13
ADD R13, R14, R15
ADD R19, R13, R10
LW R2, R3
ADD R12, R16, R19
LW R5, R2
ADD R15, R20, R21

Problem #6 (20 Points): Assume architecture I2OI from lecture.
Draw the state of the scoreboard when instruction 3 is in the I (Issue) stage of the pipeline.
0: MUL R6, R7, R8
1: ADD R9, R6, R11
2: MUL R7, R1, R2
3: LW R10, R12