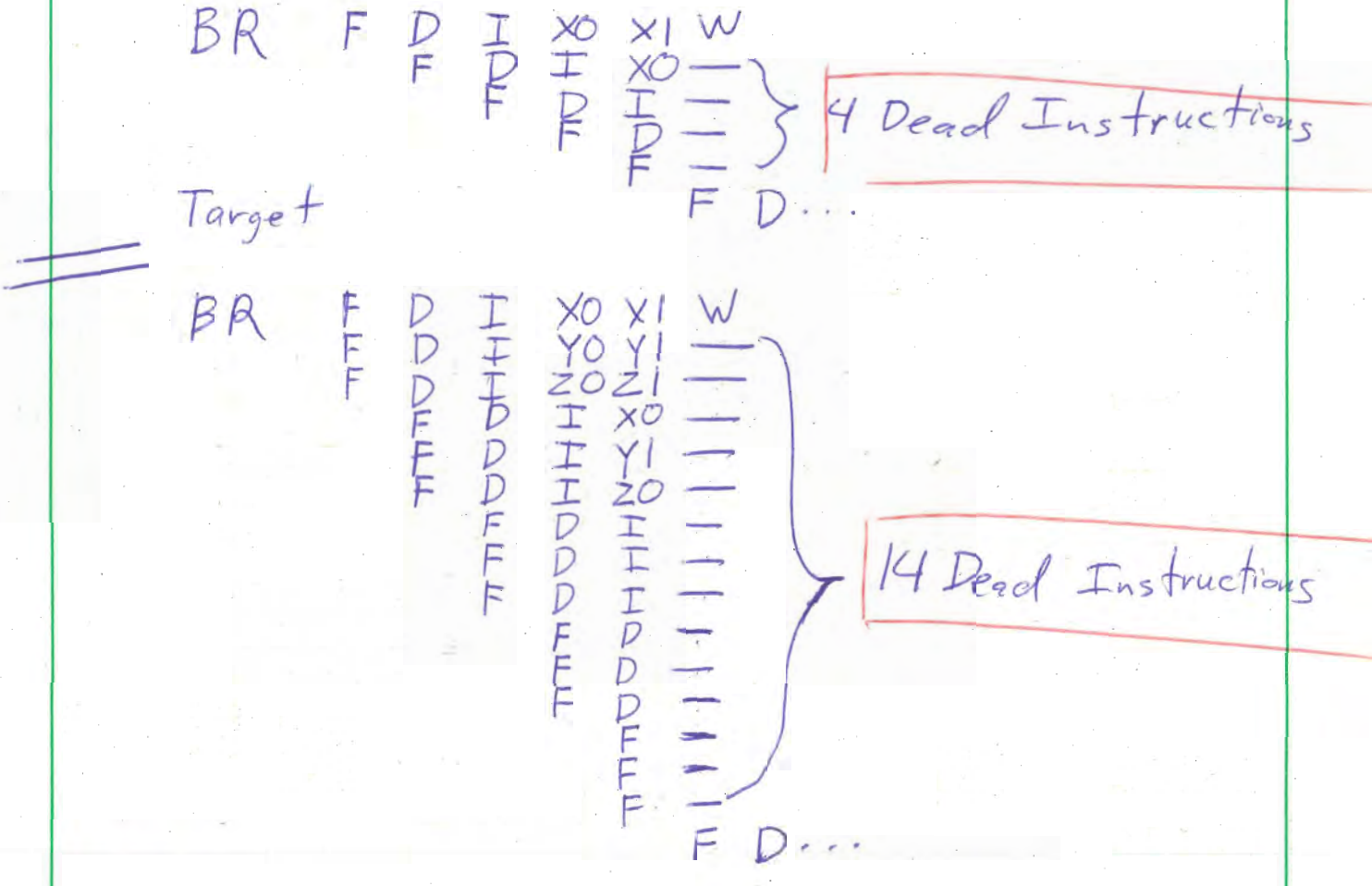
Problem 1)

```
ADD  R5, R6, R7
SUB  R6, R7, R8
LW   R10, 0(R6)
ADDIU R12, R13, 1
LW   R15, 4(R6)
LW   R15, 4([redacted]R15)
ADD  R6, R9, R10
ADD  R8, R10, 11
```

```
F  D  X0 X1 W
F  D  Y0 Y1 W
   F  D  Y0 Y1 W
   F  D  X0 X1 W
      F  D  J0 Y1 W
      F  D  D  D  Y0 Y1 W
      [redacted] F  D  D  D  X0 X1 W
         F  F  F  D  X0 X1 W
```

Problem #2)

Single Issue



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Problem 3)

a) - the Exceptional Program Counter (EPC) gets loaded with the PC of the interrupted instruction.

(If we are in a branch delay slot, EPC ← PC - 4)

- The Cause register gets loaded with the reason for the interrupt
- The Exception Level status register is set to '1' to disable further interrupts

EXL ← 1

b) R5, R8, R10

c) PC ← EPC
EXL ← 0

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Problem 4)

If Address Exception on the Instruction address and ALU Overflow happens, the Instruction address exception takes precidence and should be loaded into the Cause register. This is because the fetched instruction is not valid if we have a problem with the address of the instruction.

If an external interrupt is pending, you can take either. The ISA can document either way, but should be consistant. If the external interrupt takes precidence then external interrupts can starve execution of the main processor which is why internal/syncronous interrupts take precidence in most ISA's. If the internal/sycronous interrupt takes precidence, the external interrupt must remain pending until it is handled.

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Problem 5)

```
MUL R6, R7, R8
ADD R9, R10, R11
ADD R11, R12, R13
ADD R13, R14, R15
ADD R19, R13, R10
LW R2, R3
ADD R12, R16, R19
LW R5, R2
ADD R15, R20, R21
```

```
F D I Y0 Y1 Y2 Y3 W C
  F D I X0 W r    C
    F D I X0 W r    C
      F D i I X0 W r  C
        F D i I X0 W r  C
          F D i I L0 L1 W r C
            F D i  I X0 W r C
              F D i  I L0 L1 W C
                F D i   I X0 W C
```

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Problem 6)

I 2 O I

```
0 MUL R6, R7, R8      F D I Y0 Y1 Y2 Y3 W C
1 ADD R9, R6, R11       F D I  I  I  I  X0 W C
2 MUL R7, R1, R2          F D  D  D  D  I  Y0 Y1 Y2 Y3 W C
3 LW  R10, R12              F  F  F  F  D  I  L0 L1 W  r  C
```

Contents of Scoreboard

R9 is pending in Functional Unit 'X' and is marked as having '0' more cycles until writeback

R7 is pending in Functional Uint 'Y' and is marked as having '4' more cycles until writeback

The rest of the registers are not pending

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