Section 31. Introduction (Part III)

HIGHLIGHTS

This section of the manual contains the following major topics:

31.1 INTRODUCTION

Part III sections of the PIC24H Family Reference Manual provide information on modules specific to the low-cost, small pin count and Digital Signal Controllers (DSCs). These devices are ideally suited for low-cost, high-performance general purpose and a variety of sensor applications.

These devices feature many advanced peripherals, such as a 10-/12-bit Analog-to-Digital Converter (ADC), Programmable Cyclic Redundancy Check (CRC), Real-Time Clock and Calendar (RTCC), and a Parallel Master Port (PMP). In addition, these devices feature Peripheral Pins Select functionality, which provides flexibility of mapping any digital peripheral functionality to any desired digital pin.

Part III sections apply to these General Purpose devices:

• PIC24HJ32GP302
• PIC24HJ32GP304
• PIC24HJ64GP202
• PIC24HJ64GP204
• PIC24HJ64GP502
• PIC24HJ64GP504
• PIC24HJ128GP202
• PIC24HJ128GP204
• PIC24HJ128GP502
• PIC24HJ128GP504

Table 31-1 provides a guide to specific information about these devices.

Table 31-1:   Family Reference Manual Information Guide

For Information About:	See This Section:
CPU	Part I, Section 2
Data Memory	Part I, Section 3
Program Memory	Part I, Section 4
Flash Programming	Part I, Section 5
Reset	Part I, Section 8
Watchdog Timer and Power-Saving Modes	Part I, Section 9
Timers	Part I, Section 11
Input Capture	Part I, Section 12
Output Compare	Part I, Section 13
Analog-to-Digital Converter (ADC)	Part I, Section 16
Universal Asynchronous Receiver Transmitter (UART)	Part I, Section 17
Serial Peripheral Interface (SPI™)	Part I, Section 18
Inter-Integrated Circuit (I^{2}C™)	Part I, Section 19
Enhanced Controller Area Network (ECAN™)	Part I, Section 21
CodeGuard™ Security	Part I, Section 23
Programming and Diagnostics	Part I, Section 24
Device Configuration	Part I, Section 25
Development Tool Support	Part I, Section 26
I/O Ports with Peripheral Pin Select	Part II, Section 30
Interrupts	Part III, Section 32
Comparator	Part III, Section 34
Parallel Master Port (PMP)	Part III, Section 35
Programmable Cyclic Redundancy Check (CRC)	Part III, Section 36
Real-Time Clock and Calendar (RTCC)	Part III, Section 37
Direct Memory Access (DMA)	Part III, Section 38
Oscillator	Part III, Section 39

31.2   REVISION HISTORY

Revision A (November 2007)

This is the initial release of this document.