Section 12. Input Capture

HIGHLIGHTS

This section of the manual contains the following major topics:

Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33E/PIC24E devices.

Please consult the note at the beginning of the **"Input Capture"** chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

12.1 INTRODUCTION

This section describes the Input Capture module and its associated operational modes. The Input Capture module is used to capture a timer value from an independent timer base upon an event on the input pin. The input capture features are useful in applications requiring frequency (time period) and pulse measurement. Figure 12-1 illustrates a simplified block diagram of the Input Capture module.

Note: Refer to the specific device data sheet for further information on the number of channels available in a particular device. All input capture channels are functionally identical. In this section, an 'x' in the register name is a generic reference to an input capture channel in place of a specific input capture channel number.

The Input Capture module has multiple operating modes. These modes are selected through the ICxCON1 register. The operating modes of the Input Capture module include:

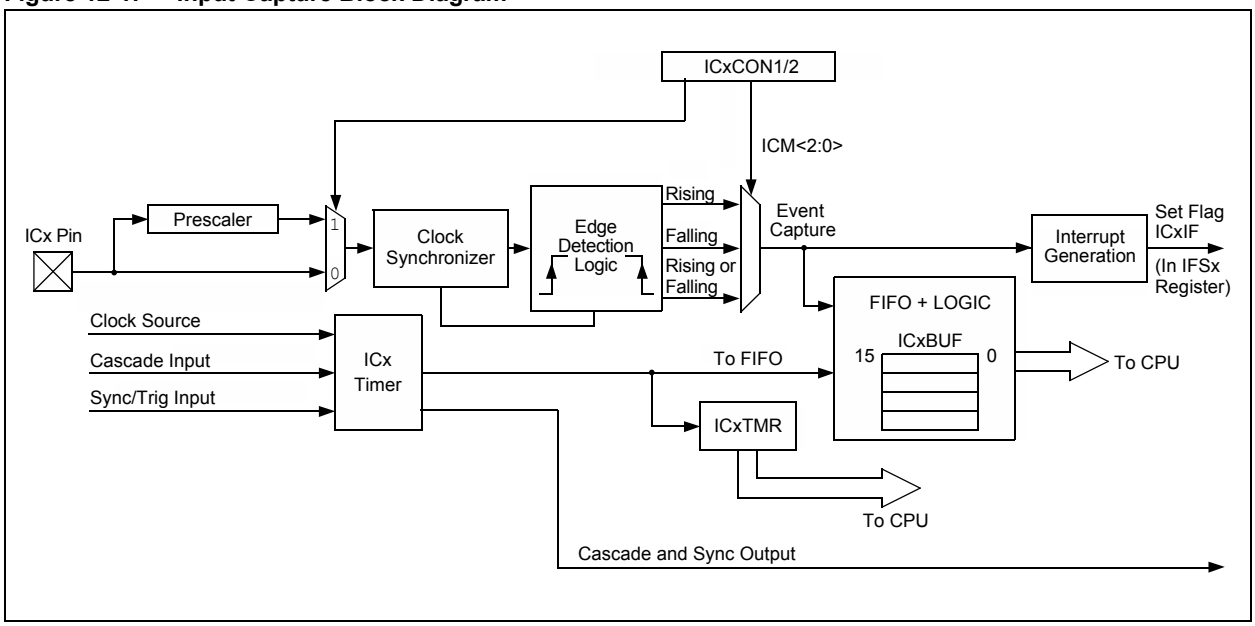
- Capture timer value on every falling edge of input applied at the ICx pin
- Capture timer value on every rising edge of input applied at the ICx pin
- Capture timer value on every 4th rising edge of input applied at the ICx pin
- Capture timer value on every 16th rising edge of input applied at the ICx pin
- Capture timer value on every rising and every falling edge of input applied at the ICx pin
- Device wake-up from capture pin during CPU Sleep and Idle modes

The Input Capture module contains a dedicated 16-bit, synchronous, up-counting timer used for the input capture function. It is the value of this timer that is written to the FIFO when a capture event occurs. In addition, the internal value may be read (with a synchronization delay) using the ICxTMR register. For more information on the ICxTMR register and its memory map details, refer to the specific device data sheet

In Cascade mode operation, the input capture timers can be grouped in pairs for the purpose of cascading them to form 32-bit timers using the cascade input and cascade output of the module. In Synchronous mode operation, the input capture timer can be synchronized with other modules using the Sync/Trig input source of the module, which is selected using the SYNCSEL<4:0> bits in the ICxCON2 register.

The Input Capture module has a four-level FIFO buffer. The number of capture events required to generate a CPU interrupt can be selected by the user-assigned application.

Figure 12-1: Input Capture Block Diagram



12.2 INPUT CAPTURE REGISTERS

Each capture channel available on the dsPIC33E/PIC24E device family has the following registers, where 'x' denotes the number of the capture peripheral:

- **ICxCON1: Input Capture X Control Register 1**
- **ICxCON2: Input Capture X Control Register 2**
- **ICxBUF: Input Capture x Buffer Register**
- **ICxTMR: Input Capture x Timer Register**

Register 12-1: ICxCON1: Input Capture x Control Register 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL<2:0>			—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	HC = Cleared by Hardware	HS = Set by Hardware	'0' = Bit is cleared
-n = Value at POR	W = Writable bit	U = Unimplemented bit, read as '0'	

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture Stop in Idle Control bit
1 = Input capture will Halt in CPU Idle mode
0 = Input capture will continue to operate in CPU Idle mode

bit 12-10 **ICTSEL<12:10>:** Input Capture Timer Select bits
111 = System clock is the counter source for capture
110 = Reserved
101 = Reserved
100 = Clock source of Timer1 is the clock source of the ICx
011 = Clock source of Timer5 is the clock source of the ICx
010 = Clock source of Timer4 is the clock source of the ICx
001 = Clock source of Timer2 is the clock source of the ICx
000 = Clock source of Timer3 is the clock source of the ICx

bit 9-7 **Unimplemented:** Read as '0'

bit 6-5 **ICI<1:0>:** Number of Captures per Interrupt Select bits
(this field is not used if ICM<2:0> = 001 or 111)
11 = Interrupt on every fourth capture event
10 = Interrupt on every third capture event
01 = Interrupt on every second capture event
00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
1 = Input capture buffer overflow occurred
0 = No input capture buffer overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
1 = Input capture buffer is not empty, at least one more capture value can be read
0 = Input capture buffer is empty

Register 12-1: ICxCON1: Input Capture x Control Register 1 (Continued)

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits

111 = Input capture functions as interrupt pin only in CPU Sleep and Idle mode (rising edge detect only, all other control bits are not applicable)
110 = Unused (module disabled)
101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
011 = Capture mode, every rising edge (Simple Capture mode)
010 = Capture mode, every falling edge (Simple Capture mode)
001 = Capture mode, every edge, rising and falling (Edge Detect mode (ICI<1:0>) is not used in this mode)
000 = Input Capture module is turned off

Register 12-2: ICxCON2: Input Capture x Control Register 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	IC32
bit 15							bit 8

R/W-0	R/W/HS-0	U-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1
ICTRIG(2)	TRIGSTAT(3)	—	SYNCSEL<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	HS = Set by Hardware	'0' = Bit is cleared
-n = Value at POR	W = Writable bit	U = Unimplemented bit, read as '0'

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **IC32:** 32-Bit Timer Mode Select bit (Cascade mode)
- 1 = ODD IC and EVEN IC form a single 32-bit Input Capture module(1)
- 0 = Cascade module operation disabled

bit 7 **ICTRIG:** Trigger Operation Select bit(2)
- 1 = Input source used to trigger the input capture timer (Trigger mode)
- 0 = Input source used to synchronize input capture timer to timer of another module (Synchronization mode)

bit 6 **TRIGSTAT:** Timer Trigger Status bit(3)
- 1 = ICxTMR has been triggered and is running
- 0 = ICxTMR has not been triggered and is being held clear

bit 5 **Unimplemented:** Read as '0'

Note 1: The IC32 bit in both the ODD and EVEN IC must be set to enable Cascade mode.

2: The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.

3: This bit is set by the selected input source (selected by SYNCSEL<4:0> bits). It can be read, set and cleared in software. Refer to **12.9.2 "Trigger Timer Operation"** for more information about this bit.

4: Do not use the ICx module as its own sync or trigger source.

5: This option should only be selected as a trigger source and not as a synchronization source.

Register 12-2: ICxCON2: Input Capture x Control Register 2 (Continued)

bit 4-0 **SYNCSEL<4:0>:** Input Source Select for Synchronization and Trigger Operation bits(4)

11111 = No sync or trigger source for ICx
11110 = IC9 module synchronizes or triggers ICx
11101 = IC6 module synchronizes or triggers ICx
11100 = Reserved
11011 = ADC1 module synchronizes or triggers ICx(5)
11010 = CMP3 module synchronizes or triggers ICx(5)
11001 = CMP2 module synchronizes or triggers ICx(5)
11000 = CMP1 module synchronizes or triggers ICx(5)
10111 = IC4 module synchronizes or triggers ICx
10110 = IC3 module synchronizes or triggers ICx
10101 = IC2 module synchronizes or triggers ICx
10100 = IC1 module synchronizes or triggers ICx
10011 = IC8 module synchronizes or triggers ICx
10010 = IC7 module synchronizes or triggers ICx
10001 = Reserved
10000 = Reserved
01111 = Timer5 synchronizes or triggers ICx
01110 = Timer4 synchronizes or triggers ICx
01101 = Timer3 synchronizes or triggers ICx
01100 = Timer2 synchronizes or triggers ICx
01011 = Timer1 synchronizes or triggers ICx
01010 = IC5 module synchronizes or triggers ICx
01001 = OC9 module synchronizes or triggers ICx
01000 = OC8 module synchronizes or triggers ICx
00111 = OC7 module synchronizes or triggers ICx
00110 = OC6 module synchronizes or triggers ICx
00101 = OC5 module synchronizes or triggers ICx
00100 = OC4 module synchronizes or triggers ICx
00011 = OC3 module synchronizes or triggers ICx
00010 = OC2 module synchronizes or triggers ICx
00001 = OC1 module synchronizes or triggers ICx
00000 = No sync or trigger source for ICx

Note 1: The IC32 bit in both the ODD and EVEN IC must be set to enable Cascade mode.

2: The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.

3: This bit is set by the selected input source (selected by SYNCSEL<4:0> bits). It can be read, set and cleared in software. Refer to **12.9.2 "Trigger Timer Operation"** for more information about this bit.

4: Do not use the ICx module as its own sync or trigger source.

5: This option should only be selected as a trigger source and not as a synchronization source.

Note:	When Timer1 synchronizes or triggers an ICx module, the Timer1 clock source must be equal to or faster than the ICx clock source for proper ICx module operation.

12.3 INITIALIZATION

When the Input Capture module is reset or is in the OFF mode (ICM<2:0> = 000), the input capture logic will:

- Reset the overflow condition flag to a logic '0'
- Reset the receive capture FIFO to the empty state
- Reset the prescale count

12.4 INPUT CAPTURE TIMER CLOCK SOURCE SELECTION

The dsPIC33E/PIC24E family devices may have one or more input capture channels. Each channel can select from one of six clock sources for its time base by using the ICTSEL<12:10> bits. Refer to the device data sheet for the specific timers that can be selected. The clock should be selected before enabling the module and should not be changed during operation.

Selection of the timer clock source is accomplished through the ICTSEL control bits (ICxCON1<12:10>). The timers can be set to use the internal clock source (FOSC/2), or use an external clock source applied at the TxCK pin with Synchronization mode enabled in the timer.

12.5 INPUT CAPTURE EVENT MODES

The Input Capture module captures the 16-bit value of the input capture timer value when an event occurs at the ICx pin. The capture events can be classified into three categories:

1. Simple Capture Event modes:
   - Capture timer value on every falling edge of input at ICx pin
   - Capture timer value on every rising edge of input at ICx pin
2. Capture timer value on every edge (rising and falling).
3. Prescaler Capture Event modes:
   - Capture timer value on every 4th rising edge of input at ICx pin
   - Capture timer value on every 16th rising edge of input at ICx pin

These Input Capture modes are configured by setting the appropriate Input Capture Mode bits (ICM<2:0>) in the ICxCON1 register (ICxCON1<2:0>).

12.5.1 Simple Capture Events

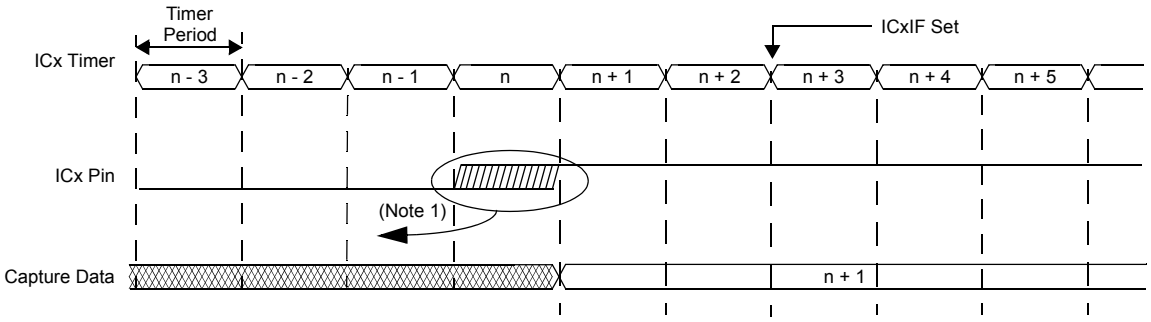
The Input Capture module can capture a timer value (dedicated timer) based on its edge selection (rising or falling as defined by the mode) of the input applied to the ICx pin. These modes are configured by setting the ICM bits (ICM<2:0>) in the ICxCON1 register (ICxCON1<2:0>) to '011' or '010', respectively. In these modes, the prescaler counter is not used. See Figure 12-2 and Figure 12-3 for timing diagrams of a simple capture event.

The input capture logic detects and synchronizes the rising or falling edge of the capture pin signal on the internal instruction clock. If the rising or falling edge has occurred, the capture module logic will write the current timer value to the capture buffer and will trigger the interrupt generation logic when the number of elapsed capture events matches the number specified by the ICI control bits (ICI<1:0>) in the ICxCON1 register (ICxCON1<6:5>). The respective Input Capture Interrupt Flag, ICxIF, is asserted two instruction cycles after the capture buffer write event.

If the capture timer increments every instruction cycle, the captured timer value will be the value that was present one or two instruction cycles after the time of the event on the ICx pin. This time delay is a function of the actual ICx edge event related to the instruction clock cycle and delay associated with the input capture logic. If the input clock to the capture time base is prescaled, then the delay in the captured value can be eliminated. For more information, see Figure 12-2 and Figure 12-4.

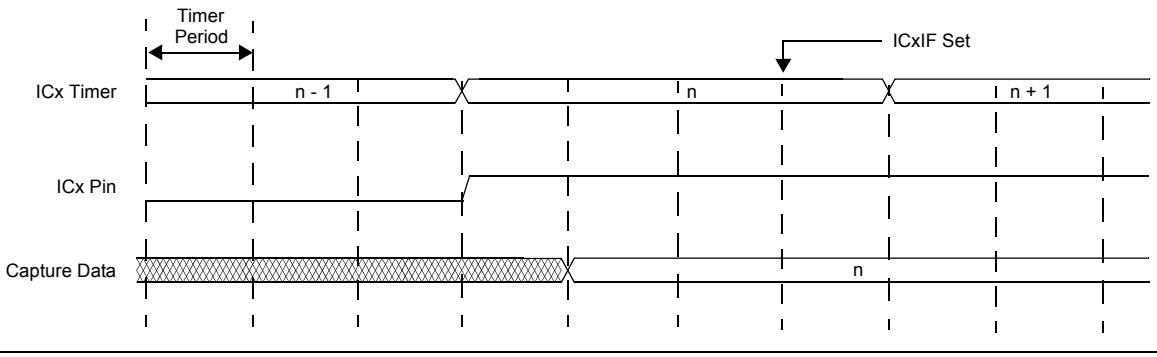
The input capture pin has minimum high time and low time specifications. For more information, refer to **12.13 "Design Tips".**

Figure 12-2: Simple Capture Timing Diagram, Time Base Prescaler = 1:1



Note 1: A capture signal edge that occurs in this region will result in a capture buffer entry value of 1 or 2 timer counts from the capture signal edge.

Figure 12-3: Simple Capture Timing Diagram, Time Base Prescaler = 1:4



12.5.1.1 CHANGING BETWEEN CAPTURE MODES

It is recommended that the user-assigned application turn off the Capture module (clear the ICM<2:0> bits (ICxCON1<2:0>)) before switching to a new mode. If the user-assigned application switches to a new capture mode, the prescaler counter will not be cleared. Therefore, at the time of switching modes, it is possible that the first capture event and its associated interrupt is generated due to a non-zero prescaler counter.

12.5.2 Prescaler Capture Events

The Capture module has two Prescaler Capture modes. The Prescaler Capture modes are selected by setting the ICM<2:0> bits (ICxCON1<2:0>) bits to '100' or '101', respectively. In these modes, the Capture module counts four or sixteen rising edge pin events before a capture event occurs.

The prescaler capture counter is incremented on every valid rising edge applied to the capture pin. The rising edge applied to the pin effectively serves as a clock to a counter. When the prescaler counter equals four or sixteen counts (depending on the mode selected), the counter will output a valid capture event signal, which is then synchronized to the instruction clock cycle.

This synchronized capture event signal triggers a capture buffer write event and signal the interrupt generation logic. The respective Input Capture Interrupt Flag, ICxIF, is asserted two instruction cycles after the capture buffer write event.

The input capture pin has minimum high time and low time specifications. For more information, refer to the Electrical Characteristics section of the specific device data sheet.

Switching from one prescale setting to another might generate an interrupt, and also the prescaler counter will not be cleared. Therefore, the first capture may be from a non-zero prescaler.

Example 12-1 provides the recommended method for switching between prescaler capture settings.

The prescaler counter is cleared, when:

- The capture channel is turned off (ICM<2:0> = 000)
- Any device Reset

The prescaler counter is not cleared, when:

- The user-assigned application switches from one active Capture mode to another

Example 12-1: Prescaler Capture Code Example

```
//The following code example will set the Input Capture1 module for interrupts on every
//second capture event; captured on every fourth rising edge. The clock source for the timer
//would be the system clock. Sync/Trig source is disabled.
// Setup Input Capture1 interrupt for desired priority level (this example assigns level 1
//priority)

IFS0bits.IC1IF = 0;       // Clear the IC1 interrupt status flag
IEC0bits.IC1IE = 1;       // Enable IC1 interrupts
IPC0bits.IC1IP = 1;       // Set module interrupt priority as 1

IC1CON1 = 0x1C24;         // Turn on Input Capture 1 Module
IC1CON2 = 0x0000;         // Turn on Input Capture 1 Module

// The following code shows how to read the capture buffer when
// an interrupt is generated.
// Example code for Input Capture 1 ISR:
unsigned int Capture1, Capture2;
void __attribute__ ((__interrupt__, no_auto_psv)) _IC1Interrupt(void)
    {
        IFS0bits.IC1IF = 0;    // Reset respective interrupt flag
        Capture1 = IC1BUF;     // Read and save off first capture entry
        Capture2 = IC1BUF;     // Read and save off second capture entry
    }
```


12.5.3 Edge Detection Mode

The Input Capture module can capture a time base count value on every rising and falling edge of the input signal applied to the ICx pin. The Edge Detection mode is selected by setting the ICM<2:0> bits (ICxCON1<2:0>) to '001'. In this mode, the prescaler capture counter is not used. For a simplified timing diagram, see Figure 12-4.

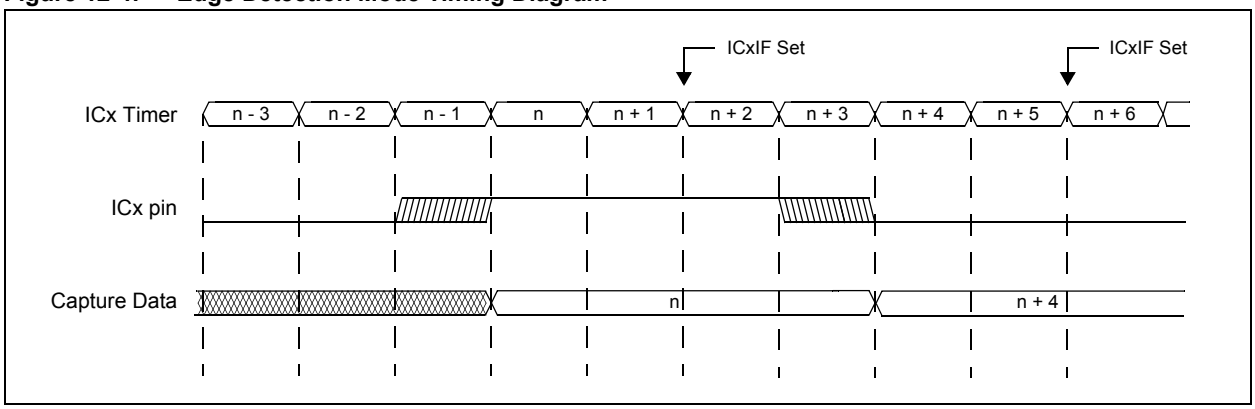
When the Input Capture module is configured for an edge detection (Edge Detection mode), the module performs these tasks:

- Set the Input Capture Interrupt Flag (ICxIF) on every edge: rising and falling.
- The interrupt for Capture mode bits, (ICI<1:0>) of the ICxCON1 register (ICxCON1<6:5>), are not used in this mode. Every capture event generates an interrupt.

As with the simple Capture Event mode, the input capture logic detects and synchronizes the rising and falling edge of the capture pin signal on the internal phase clocks. If the rising or falling edge has occurred, the capture module logic will write the current timer count on to the capture buffer and signal the interrupt generation logic. The respective Input Capture Interrupt Flag, ICxIF, is asserted two instruction cycles after the capture buffer write event.

The captured timer count value will be 1 or 2 timer counts after the occurrence of the edge at the ICx pin (see Figure 12-4).

Figure 12-4: Edge Detection Mode Timing Diagram



12.6 CAPTURE BUFFER OPERATION

Each capture channel has a FIFO buffer associated with it. The ICxBUF register is memory mapped and provides access to the FIFO. When the Input Capture module is reset (ICxCON1<2:0> = 000), the input capture logic performs these tasks:

- Clear the overflow condition flag (that is, clear ICOV (ICxCON1<4>) to '0')
- Reset the capture buffer to the empty state (clears ICBNE (ICxCON1<3>) to '0')

Reading the FIFO buffer under the following conditions will lead to indeterminate results:

- The Input Capture module is first disabled, and at some later time re-enabled
- A FIFO read is performed when the buffer is empty
- After a device Reset, before a capture event has occurred

There are two status flags that provide status on the FIFO buffer:

- ICBNE (ICxCON1<3>): Input Capture Buffer Not Empty
- ICOV (ICxCON1<4>): Input Capture Overflow

12.6.1 Input Capture Buffer Not Empty (ICBNE)

The ICBNE read-only status bit (ICxCON1<3>) will be set on the first input capture event and remain set until all the capture events have been read from the capture buffer. For example, if three capture events have occurred, then three reads of the capture buffer are required before the ICBNE (ICxCON1<3>) bit gets cleared. If four capture events occur, then four reads are required to clear the ICBNE (ICxCON1<3>) bit. After each read, the remaining words will be allowed to move to the next available top location. Because the ICBNE reflects the capture buffer state, the ICBNE status bit will be cleared during a device Reset.

12.6.2 Input Capture Overflow (ICOV)

The ICOV read-only status bit (ICxCON1<4>) will be set when the capture buffer overflows. In the event that the buffer is full with four capture events, and a fifth capture event occurs prior to reading of the buffer, an overrun condition will occur. The ICOV (ICxCON1<4>) bit will be set to logic '1' and the respective capture event interrupt will not be generated. In addition, the fifth capture event is not recorded and subsequent capture events will not alter the current buffer contents.

To clear the overrun condition, the capture buffer must be read four times. Upon the fourth read, the ICOV (ICxCON1<4>) status flag will be cleared and the capture channel will resume normal operation.

Clearing of the overflow condition can be accomplished in the following ways:

- Set ICM<2:0> bits (ICxCON1<2:0>) = 000
- Read the capture buffer until ICBNE (ICxCON1<3>) = 0
- Any device Reset

A FIFO overflow occurs under the following conditions:

- ICM<2:0> is not equal to '000' (not off)
- ICM<2:0> is not equal to '110' (not disabled)
- ICM<2:0> is not equal to '001' (not in Edge Detect Mode)
- (Idle_mode = 0 or ICSIDL = 0 or ICM<2:0> is not equal to '111')
- FIFO is full
- Capture event has occurred

Note:	When ICI<1:0> = 00 or ICM<2:0> = 001, interrupts occur and the ICOV bit remains clear even after a buffer overflow has occurred.

12.6.2.1 ICOV AND INTERRUPT-ONLY MODE

The Input Capture module can also be configured to function as an external interrupt pin. For this mode, the ICI<1:0> bits (ICxCON1<6:5>) must be cleared to '00'. Interrupts will be generated independent of buffer reads.

12.7 INPUT CAPTURE INTERRUPTS

The Input Capture module can generate interrupts based upon a selected number of capture events. A capture event is defined as a write of a time base value into the capture buffer. This setting is configured by the control bits, ICI<1:0> (ICxCON1<6:5>).

Except for the case when ICI<1:0> = 00 or ICM <2:0> = 001, no interrupts will be generated until a buffer overflow condition is removed (see **12.6.2 "Input Capture Overflow (ICOV)"**).

When the capture buffer is emptied, either by a Reset condition or a read operation, the interrupt count is reset. This allows for the resynchronization of the interrupt count to the FIFO entry status.

12.7.1 Interrupt Control Bits

Each input capture channel has Interrupt Capture Flag bits (ICxIF), Interrupt Capture Enable bits (ICxIE) and Interrupt Capture Interrupt Priority bits (ICxIP<2:0>).

12.8 INPUT CAPTURE OPERATION IN POWER-SAVING STATES

12.8.1 Input Capture Operation in Sleep Mode

When the device enters Sleep mode, the system clock is disabled. In Sleep mode, the Input Capture module can only function as an external interrupt source and the capture result is not valid. This mode is enabled by setting control bits, ICM<2:0> = 111. In this mode, a rising edge on the capture pin will generate a device wake-up from Sleep condition. If the respective module interrupt bit is enabled, and the module priority is of the required priority, an interrupt will be generated; an active timer is not required.

In the event the capture module is configured for a mode other than ICM<2:0> = 111, and the dsPIC33E/PIC24E device enters Sleep mode, no external pin stimulus, rising or falling, will generate a wake-up condition from Sleep mode.

12.8.2 Input Capture Operation in Idle Mode

When the device enters Idle mode, the system clock sources remain functional and the CPU stops executing code. The ICSIDL bit (ICxCON1<13>) selection will determine if the module will stop in Idle mode or continue to operate in Idle mode.

If ICSIDL = 0 (ICxCON1<13>), the module will continue operation in Idle mode. Full functionality of the Input Capture module is provided (including the 4:1 and 16:1 prescaler capture settings) as defined by the ICM<2:0> control bits (ICxCON1<2:0>). These modes require that the selected timer is enabled during Idle mode as well.

If the Input Capture mode is configured for ICM<2:0> = 111, the input capture pin will serve only as an external interrupt pin. In this mode, a rising edge on the capture pin will generate a device wake-up from Idle mode. A capture time base does not have to be enabled. If the respective module interrupt enable bit is set, and the user-assigned application priority is greater than the current CPU priority level, an interrupt will be generated.

If ICSIDL = 1 (ICxCON1<13>), the module will stop in Idle mode. The module will perform the same functions when stopped in Idle mode as for Sleep mode (see **12.8.1 "Input Capture Operation in Sleep Mode"**).

12.8.3 Device Wake-up on Sleep or Idle Mode

An input capture event can generate a device wake-up or interrupt, if enabled, if the device is in Idle or Sleep mode.

Independent of the timer being enabled, the Input Capture module will wake-up from Sleep or Idle mode when a capture event occurs if the following are true:

- Input Capture Mode bits, ICM<2:0> = 111 (ICxCON1<2:0>)
- The Interrupt Capture Enable bit (ICxIE) is asserted.

This same wake-up feature will interrupt the CPU if the respective interrupt is enabled (ICxIE = 1) and is of the required priority.

This wake-up feature is useful for including additional external pin interrupts. The following conditions are true when the Input Capture module is used in this mode:

- The prescaler capture counter is not utilized while in this mode
- The ICI<1:0> bits (ICxCON1<6:5>) are not applicable

12.8.4 Doze Mode

Input capture operation in Doze mode is the same as in normal mode. When the device enters Doze mode, the system clock sources remain functional and the CPU may run at a slower clock rate. For more information, refer to **Section 9. "Watchdog Timer and Power-Saving Modes"** of the *"dsPIC33E/PIC24E Family Reference Manual"*.

12.8.5 Selective Peripheral Module Control

The Peripheral Module Disable (PMD) registers provide a method to disable the Input Capture module by stopping all clock sources supplied to it. When the module is disabled through the appropriate PMD control bit, it is in a minimum power consumption state. The control and status registers associated with the module will also be disabled, hence any write to these registers will have no effect, and read values will be invalid and return zero. For more information, refer to **Section 9. "Watchdog Timer and Power-Saving Modes"** of the *"dsPIC33E/PIC24E Family Reference Manual"*.

12.9 INPUT CAPTURE TIMER FUNCTIONALITY

The Input Capture module contains a 16-bit synchronous up-counting timer used for the capture function. This timer has the following functionality:

- Synchronous operation – The timer rolls over when it reaches FFFFh or when the Sync/Trig input is enabled.
- Triggered operation (hardware and/or software) – The timer starts operation based on a hardware or software trigger and can be cleared and stopped by software.
- Cascaded operation (32-bit Timer mode) – The EVEN timer will increment when the associated ODD timer rolls over, and the ODD timer increments every timer clock period when enabled.

12.9.1 Synchronous Timer Operation

Synchronous operation of the timer is enabled when:

- ICTRIG = 0
- A valid synchronization input is selected using the SYNCSEL<4:0> bits

In synchronous operation, the TRIGSTAT bit has no function. The timer can be synchronized with other modules using the Sync/Trig input source of the module, which is selected using the SYNCSEL<4:0> bits.

Figure 12-5 and Figure 12-6 show the timer operation in conjunction with a Sync/Trig input source. When a valid synchronization input is selected using Sync/Trig input source bits, the timer increments on every timer clock (selected by the ICTSEL<12:10> bits). When the selected Sync/Trig input source = 1, the timer will be cleared on the next rising edge of the timer clock. As long as the Sync/Trig input source = 1, the timer will remain cleared.

When the Sync/Trig input source is negated, the timer will resume incrementing on the next positive edge of the timer clock. The Sync/Trig input is driven by the synchronization output of another module (typically, an Output Compare or Input Capture module).

When initializing timers that have synchronous timer operation enabled, the timer being used as the source of synchronization must be enabled last.

Note 1: Synchronized timers must select the same clock source to ensure proper function.

2: When initializing timers that have synchronous timer operation enabled, the timer being used as the source of synchronization must be enabled last.

3: The Sync/Trig input must be synchronous to the timer clock to ensure proper operation.

Figure 12-5: Synchronous Operation Timing (ICTRIG = 0)

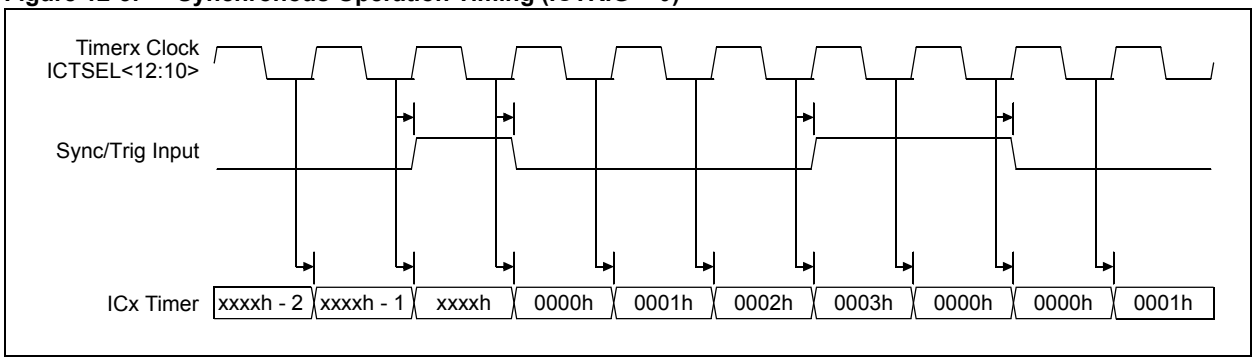
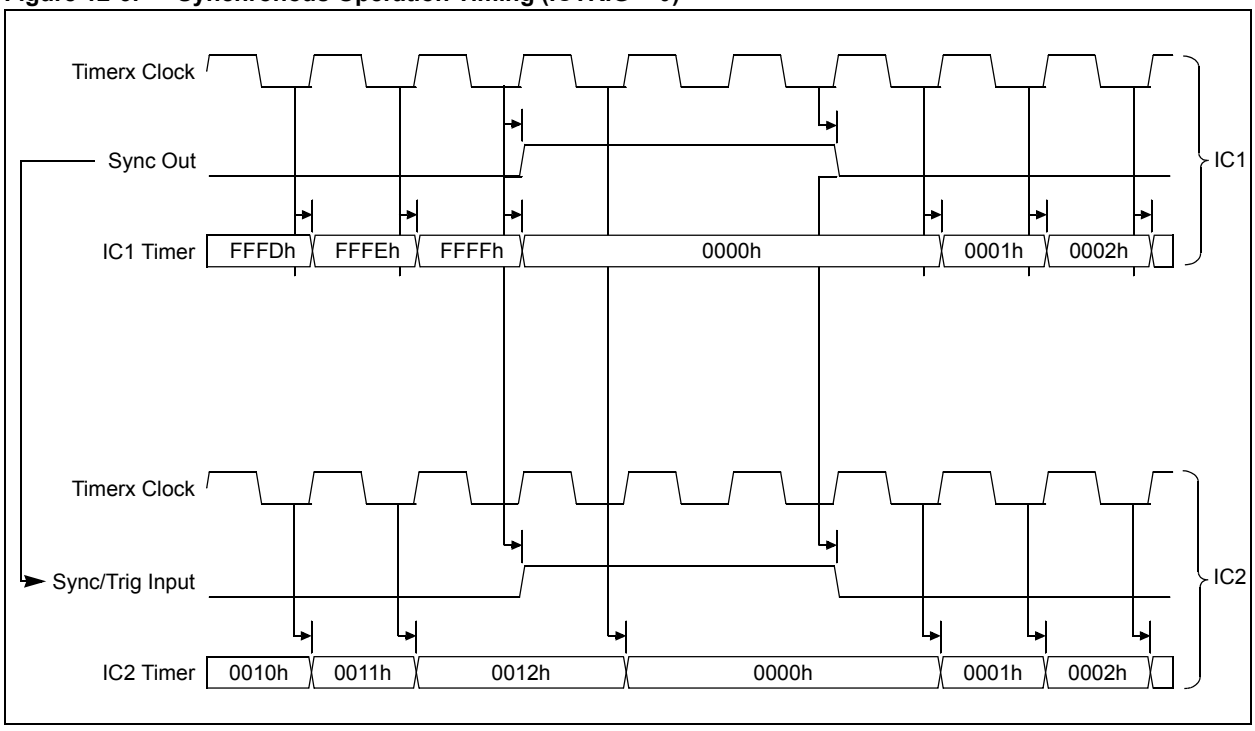


Figure 12-6: Synchronous Operation Timing (ICTRIG = 0)



12.9.2 Trigger Timer Operation

Triggered operation of the timer is enabled when ICTRIG = 1 and a valid Sync/Trig input source is selected using the SYNCSEL<4:0> bits. During triggered operation, the TRIGSTAT bit is set by hardware or software and can be cleared by software.

The TRIGSTAT bit has the following functions during trigger operation:

- TRIGSTAT = 0
  - Timer is held in Reset
- TRIGSTAT = 1
  - Timer released from Reset
  - Timer increments on every positive clock

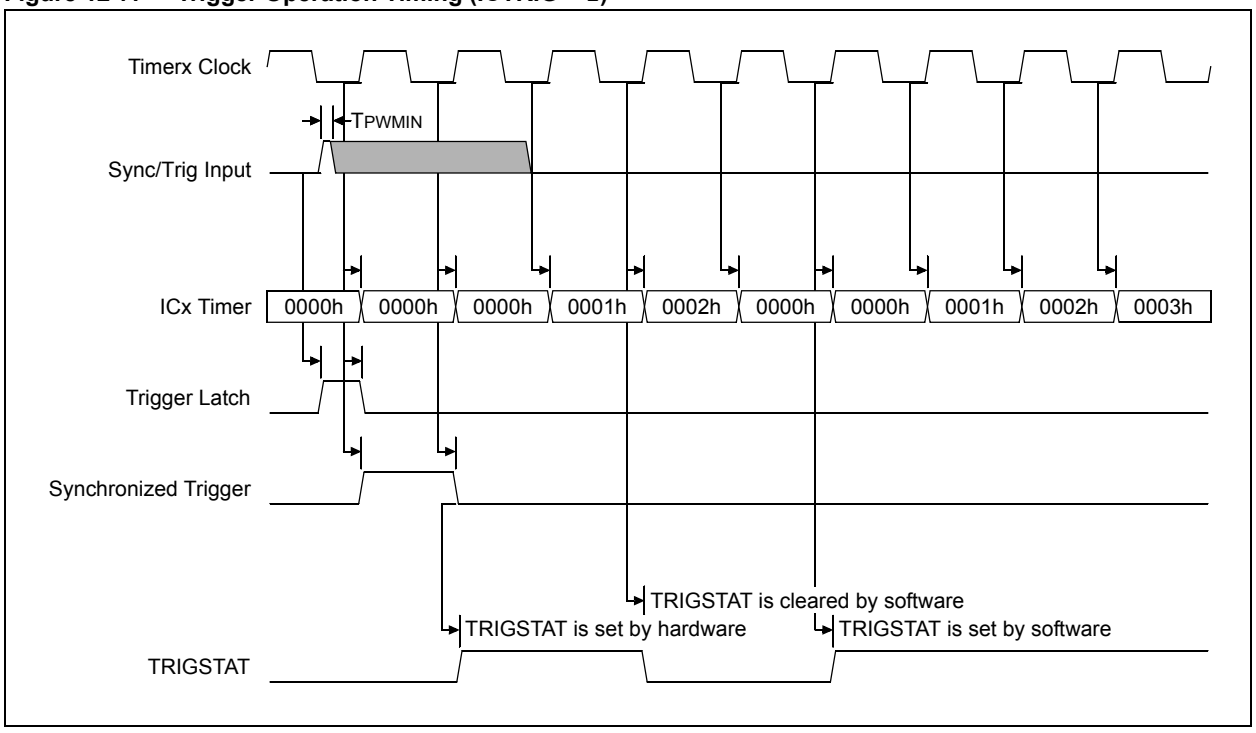
Trigger operation is shown in Figure 12-7. When triggered timer operation is enabled, the timer will be held in a cleared state. It will remain in this cleared state until a trigger occurs on the selected Sync/Trig input source (SYNCSEL<4:0>), at which point, the TRIGSTAT bit is set. In addition to being set by hardware, the TRIGSTAT bit may also be set in software. After the TRIGSTAT bit is set, the timer is released from Reset and starts running. When the TRIGSTAT bit is cleared in software, the timer is reset to 0000h and is ready for another Sync/Trig input (SYNCSEL<4:0>) assertion.

When TRIGSTAT = 0, the timer is held in Reset (0000h), but the input capture functionality is still active. If an input capture event occurs during this time, the value of the timer (0000h) will be captured into the FIFO buffer.

When setting up the Input Capture module, make sure to set all other input capture configurations and the TRIGSTAT bit is still zero ('0') before changing the ICM<2:0> bits from zero ('0') to enable the Input Capture module. Trigger functionality is based on the rising edge of the Sync/Trig input rather than the level trigger.

Note:	The Sync/Trig input must be synchronous to the timer clock and must be a minimum of one timer clock cycle in width to ensure proper operation.

Figure 12-7: Trigger Operation Timing (ICTRIG = 1)

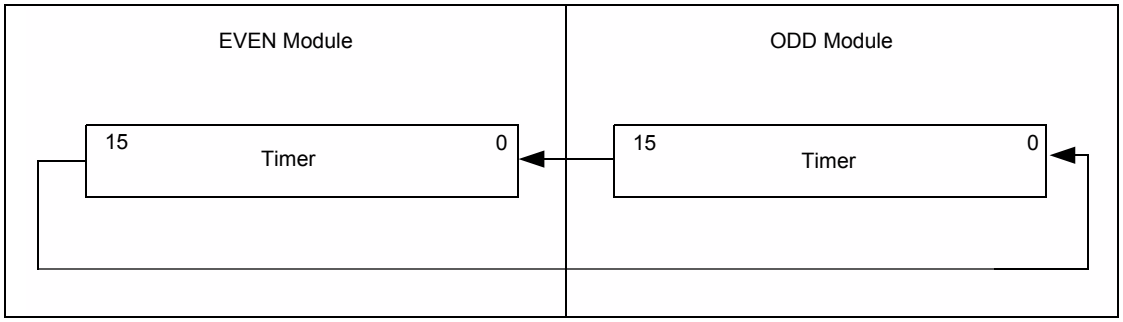


12.9.3 Cascaded Timer Operation (32-Bit Timer Mode)

Cascaded operation of the timer is enabled when IC32 = 1. Timers can be grouped in pairs for the purpose of cascading them to form 32-bit timers using the cascade input and cascade output of the module. They are grouped as ODD and EVEN pairs (1-2, 3-4, 5-6, 7-8 and so on). When cascading, the ODD timer will be the Least Significant 16 bits and the EVEN timer will be the Most Significant 16 bits.

Cascade operation is illustrated in Figure 12-8. As long as cascade input is low, the timer will not be incremented. When the cascade input is high, the timer will be incremented on the rising edge of the timer clock.

Figure 12-8: Cascaded Timer Operation



Note 1: When operating two timers in a cascade configuration, the modules must use the same clock source.
2: When cascading timers, both timers must have IC32 = 1.
3: When initializing cascaded modules, the module being used as the source of cascade_out (that is, Least Significant 16 bits) should be enabled last.

While cascading, the cascade_out from the ODD Input Capture module will be connected to cascade_in of the EVEN Input Capture module. When the ICx timer of the ODD module reaches FFFFh, it will assert the cascade_out, which will cause the ICx timer of the EVEN module to be incremented in the next clock cycle.

12.9.3.1 TIMER CONFIGURATION

Based on the timer functionality as described in Figure 12-8, there are many different configurations that the timer can be operated in:

- **Normal Configuration** – The timer operates as a standard up-counter, rolling over to 0000h only when it reaches FFFFh. This mode is set by IC32 = 0, ICTRIG = 0 and SYNCSEL<4:0> = 0h. In this mode, the TRIGSTAT bit is unused.
- **Synchronous Configuration** – The timer may be synchronized with another timer such that both timers roll over simultaneously. This mode is set by IC32 = 0, ICTRIG = 0 and SYNCSEL <4:0> is not equal to 0h. In this mode, the TRIGSTAT bit is unused.
- **Software Triggered Configuration** – The timer may be triggered by software to start the timer operation. This mode is set by IC32 = 0, ICTRIG = 1 and SYNCSEL<4:0> = 0h. In this mode, the TRIGSTAT bit is used.
- **Hardware/Software Triggered Configuration** – The timer may be triggered by a trigger outside the module (for example, comparator) or by software to start the timer operation. This mode is set by IC32 = 0, ICTRIG = 1 and SYNCSEL<4:0> is not equal to 0h. In this mode, the TRIGSTAT bit is used.
- **Normal Cascaded Configuration** – The timer may be cascaded with another timer so that two 16-bit timers can be combined to form a single 32-bit timer. This mode is set by IC32 = 1, ICTRIG = 0 and SYNCSEL<4:0> = 0h. In this mode, the TRIGSTAT bit is unused.
- **Synchronous Cascaded Configuration** – The timer may be cascaded with another timer to form a 32-bit timer that is synchronized with another 32-bit timer. This mode is set by IC32 = 1, ICTRIG = 0 and SYNCSEL<4:0> is not equal to 0h. In this mode, the TRIGSTAT bit is unused.

- **Software Triggered Cascaded Configuration** – The timer may be cascaded with another timer to form a 32-bit timer that may be triggered by software to start the timer operation. This mode is set by IC32 = 1, ICTRIG = 1 and SYNCSEL<4:0> = 0h. In this mode, the TRIGSTAT bit is used.
- **Hardware/Software Triggered Cascaded Configuration** – The timer may be cascaded with another timer to form a 32-bit timer that may be triggered from outside the module itself (by comparator and so on), or by software to start the timer operation. This mode is set by IC32 = 1, ICTRIG = 1 and SYNCSEL<4:0> is not equal to 0h. In this mode, the TRIGSTAT bit is used. All other combinations of Configuration bits are undefined and should not be used.

12.10 I/O PIN CONTROL

When the Capture module is enabled, the user must ensure that the I/O pin direction is configured for an input by setting the associated TRIS bit. The pin direction is not set when the capture module is enabled. Furthermore, all other peripherals multiplexed with the input pin must be disabled.

12.11 INPUT CAPTURE OPERATION WITH DMA

Some dsPIC33E/PIC24E family devices include a Direct Memory Access (DMA) module, which allows data to be transferred from the Input Capture module to data memory without CPU intervention. Refer the specific device data sheet to see if DMA is present on your particular device. For more information on the DMA module, refer to **Section 22. "Direct Memory Access (DMA)"** of the *"dsPIC33E/PIC24E Family Reference Manual"*.

When the Input Capture module and DMA channel are configured, the Input Capture module issues a DMA request for every capture event. The DMA transfers data from the Input Capture Buffer (ICxBUF) register into RAM, and issues a CPU interrupt after a predefined number of transfers.

The DMA channel must be initialized with the following:

- The DMA Request Source Selection (IRQSEL<7:0>) bits in the DMA Request (DMAxREQ<7:0>) register must select the DMA transfer request from Input Capture module
- The DMA Channel Peripheral Address (DMAxPAD) register must be initialized with the address of the Input Capture Buffer (ICxBUF) register
- The Transfer Direction (DIR) bit in DMA Control (DMAxCON<13>) register must be cleared. In this condition, data is read from the peripheral and written to the dual port DMA memory

In addition, the input capture interrupt bits must be cleared (ICI<1:0> = 00) to generate a DMA request for every capture event.

Example 12-2 provides sample code that transfers the capture values to RAM with DMA.

DMA Channel 0 is set up for the Input Capture module with the following configuration:

- Transfer data from the Input Capture module to RAM
- One-shot operating mode
- Register Indirect with Post-Increment addressing
- Single buffer
- 256 transfers per buffer
- Transfer words

Example 12-2: Input Capture with DMA

```
//Define Buffer in DMA RAM as global variable:
__eds__ unsigned int BufferA[256] __attribute__((space(eds)));

//Initialize Input Capture Module:

    IC1CON1bits.ICM = 0b000;      // Disable Input Capture 1 module
    IC1CON1bits.ICTSEL = 7;       // Select system clock as the IC1 Time base
    IC1CON1bits.ICI = 0b00;       // Interrupt on every capture event
    IC1CON1bits.ICM = 0b001;      // Generate capture event on every edge
    IC1CON2 = 0;                  // No sync or trigger source for IC1

//Set up DMA for Input Capture:

    DMA0CONbits.AMODE = 0b00;     // Register indirect with post increment
    DMA0CONbits.MODE = 0b01;      // One Shot, Ping-Pong mode Disabled
    DMA0CONbits.DIR = 0;          // Peripheral to RAM
    DMA0PAD = (int)&IC1BUF;       // Address of the capture buffer register
    DMA0REQ = 1;                  // Select IC module as DMA request source
    DMA0CNT = 255;                // Number of words to buffer

    DMA0STAH = __builtin_dmapage (&BufferA);
    DMA0STAL = __builtin_dmaoffset (&BufferA);

    IFS0bits.DMA0IF = 0;          // Clear the DMA interrupt flag bit
    IEC0bits.DMA0IE = 1;          // Enable DMA interrupt enable bit
    DMA0CONbits.CHEN = 1;


//Set up DMA Interrupt Handler:

    void __attribute__((__interrupt__, no_auto_psv)) _DMA0Interrupt(void)
    {
    // Process the captured values
    IFS0bits.DMA0IF = 0; // Clear the DMA0 Interrupt Flag
    }
```

12.12 REGISTER MAPS

A summary of the registers associated with the dsPIC33E/PIC24E Input Capture module is provided in Table 12-1.

Table 12-1: Input Capture Register Map

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ICxBUF	Input Capture x Buffer Register																xxxx
ICxCON1	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM2	ICM1	ICM0	0000
ICxCON2	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D
ICxTMR	Input Capture x Timer																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

12.13 DESIGN TIPS

Question 1: ***Can the Input Capture module be used to wake the device from Sleep mode?***

Answer: Yes. When the Input Capture module is configured to ICM<2:0> = 111 and the respective channel Interrupt Capture Enable bit is asserted (ICxIE = 1), a rising edge on the capture pin will wake the device from Sleep mode (see **Section 12.8 "Input Capture Operation in Power-Saving States"**).

12.14 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33E/PIC24E device family, but the concepts are pertinent and can be used with modification and possible limitations. The current application notes related to the Input Capture are:

Title	Application Note #
No application notes are available.	

Note: Visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the dsPIC33E/PIC24E family of devices.

12.15 REVISION HISTORY

Revision A (November 2008)

This is the initial released revision of this document.

Revision B (July 2010)

This revision includes the following updates:

- Updated the Input Capture Block Diagram (Figure 12-1)
- Updated the bit value definitions for the ICTSEL<12:10> bits in the ICxCON1 register (Register 12-1)
- Added Note 5 and updated the bit value definitions for the SYNCSEL<4:0> bits in the ICxCON2 register (Register 12-2)
- Added a shaded note after the ICxCON2 register
- Updated the IC1 Timer values in the Synchronous Operating Timing (ICTRIG = 0) diagram (Figure 12-6)
- Updated the Input Capture With DMA code example (Example 12-2)
- Updated the ICxCON2 All Resets value in the register map (Table 12-1)
- Additional minor formatting updates were incorporated throughout the document

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